















How it works

- The memory is split between nodes
- Clearly the access to a remote node's local memory is slower
- A request from one of the nodes has to either go to the bus, possibly cached, or to the local memory
- Caches need to be up-to-date all the time

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MP synchronization

- Appropriate synchronization procedure are needed
 - Disabling interrupt doesn't work
- TSL instruction, locking also the BUS while reading/writing atomically
 - Lock_bus
 - Read, Write
 - Unlock_bus
- Otherwise, if the bus doesn't support TSL, there's always Peterson's solution

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Hyper-threading

- PIV processors
- Execute 2 threads at once
- Since many instructions do different things they also use different subset of the CPU
- Idea! Why not keep most of the CPU always busy by allowing the execution of another thread
- This is clearly all done in hardware

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